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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	
Li, Bin	:	Examiner: Rizk, Samir Wadie
Serial No.: 10/046,639	:	Group Art Unit: 2133
Filed: 10/26/2001	:	

For: Optimal Bit Allocation System for Reed-Soloman Coded Data

APPEAL REPLY BRIEF

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I. RESPONSE TO EXAMINER'S ANSWER BRIEF

The Examiner in his answer has restated his rejection of the claims (p. 1-7) and added two responses to the Applicant's Appeal. This Reply Brief addresses these two additional arguments, namely 1) a newly cited passage in Locke allegedly supports the Examiner's rejection (paragraphs 1-2) and 2) a further argument attempting to bolster Examiner's conclusion as to why Locke is enabling (paragraphs 3-4).

1. Examiner's Arguments in Paragraphs 1-3

The Examiner has continued his rejection of Claims 1-24 under 35 USC 102(e) as being anticipated by Locke et al. US Patent No. 6598188 B1 (hereinafter "Locke"). This rejection is respectfully traversed. The Applicant reincorporates all of the arguments made in the Appeal Brief and further argues as follows:

The Examiner has cited a new portion of Locke as allegedly supporting his earlier rejection. The Examiner cites Column 7, lines 19-28 as allegedly showing calculation of coding gain in the program as recited in the claims, "[Locke shows] in detail an iterative method of correction power to determine code-word length." (Page 8, paragraph 2 of the Examiner's answer). This position is unsupportable and incorrect, and instead supports Applicant's position that the patent is non-enabling as even an authority such as the Examiner cannot determine the meaning of the invention from the limited written description and/or program listing.

Tellingly, the Examiner's reference is to programming lines and not to written explanation of the program in the detailed description as there is no correlating explanation or enabling disclosure of the meaning of this code. However, a detailed review of the code and comparison to other sections of the patent shows that this section does not calculate "coding

gain" or any type of electrical power requirements for transmitting data, but in fact merely refers to the number of bytes that are potentially correctable in a particular error correction scheme, given a certain number of parity bytes, along with other factors such as use trellis coding and interleave depth.

A review of the progeam in lines 19-43 shows that "correcting power" is merely the parity bytes ("R") divided by an integer, which calculates the number of correctable bytes for a given error correction scheme. There is no showing of how electrical power requirements could be determined from such equation, and the divisor is certainly not a conversion factor from parity bytes to electrical power. Further examination shows that the integer divided into "R" to get correcting power is based on various error coding schemes, such as the use of trellis coding (See col 7, lines 21-24), where trellis coding gives approximately four times as much potential error correction ("(parity bytes per codeword)/16" vs. "(parity bytes per codeword)/4"). Column 7, lines 31-43 show the effect of potential error correction based on trellis coding and interleave depth resulting in a divisor of 2-16 pending on the interleave depth and trellis coding. It is unlikely that changing the interleave depth has such a direct correlation with the amount of electrical power that the circuit requires ("coding gain").

This definition of "correcting power" as correctable error bytes is further verified and supported elsewhere in the limited written description of the invention. The program at column 7, lines 28-29 shows the use of the "correcting power" and the gap ("mean squared error") to determine a potential codeword size from table parity_tbl. This table is also described in Column 4, lines 7-29. The table is defined as having variables gap and "t". "Gap" is defined as the mean squared error (MSE) (See column 2, lines 37-38), and "t" is the number of bytes correctable by Reed-Solomon error correction coding (See Column 3, lines 27-30), namely R/2 in the example.

As best understood from the specification, the variables are used to determine a codeword size "N." (See column 4, lines 15-21) Since this table is the same table used in the program, it can only be concluded that the "correction power" determined in the program and entered into the table is the same as "t," which is the number of correctable bytes for the error correction scheme, with R/2 being an example of t. Therefore "correction power" is not a calculation of electrical power, but a term for the "power" of the error correction scheme to fix a certain number of errors. This is in no way "coding gain."

See also column 27, lines 9-15 which define the table parity_tbl as "a two dimension table of maximum size Reed-Solomon codewords ... indexed by the margin and the correcting power of the Reed-Solomon code." Thus, the Applicant continues to state that the Locke does not teach calculation of the coding gain, and especially does not use coding gain as a variable. Locke merely, in the cited section, calculates the number of bytes correctable based on the number of parity bytes and the particular correction scheme. For at least these reasons, and the reasons provided in the Appeal Brief, the rejection cannot stand.

2. Examiner's Arguments in Paragraphs 4-5

The Examiner in his Answer Brief further attempts to bolster his conclusion that Locke provides an enabling disclosure of the Applicant's invention, stating that "By referring to adjusting coding gain in the manner Locke does, Locke implies that those of ordinary skill in the art would know how to adjust the coding gain and therefore no further explanation is needed to enable dynamic selection of error corrective parameters via coding gain." This is circular logic and certainly contrary to the case law cited in the Appeal Brief. The Applicant reiterates and reincorporates those cites in the Appeal Brief herein, for example, see *Advanced Display Systems*

Inc. v. Kent State University, 54 USPQ 2d 1673, 1679 (Fed. Cir. 2000)("Accordingly, invalidity by anticipation requires that the four corners of *a single, prior art document* describe every element of the claimed invention, expressly or inherently, such that *a person of ordinary skill in the art could practice the invention without undue experimentation.*")(emphasis added); See also, *PPG Industries, Inc. v. Guardian Industries Corp.*, 37 USPQ 2d 1618, 1624 (Fed. Cir. 1996)("To anticipate a claim, a reference must disclose every element of the challenged claim and *enable one skilled in the art to make the anticipating subject matter.*")(emphasis added) Also, "*Inherency, however, may not be established by probabilities or possibilities.* The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Oelrich,* 666 F.2d 578, 581, 212 USPQ 323, 326 (CCPA 1981)(emphasis added).

There is no simply no teaching of how to adjust coding gain, nor is there even evidence that Locke himself was aware of the desirability or capability to adjust coding gain as recited in the claims ("It *might* be possible to adjust the coding gain for this factor." Col. 5, lines 11-13. Emphasis Added). In the section cited by the Examiner, namely Col. 1, lines 40-50, there is no description that coding gain is an important consideration, and in fact, Locke teaches away, stating that "The variables of interest are the number of bits and proportion of total power allocated to each sub-carrier. Maximize the total bit rate by choosing the values of these variables to approximately equalize the bit error rates among the sub-carriers." Id. Signal power and noise power are not the same as coding gain, and one of ordinary skill in the art examining signal noise and noise power would not necessarily consider coding gain.

Therefore the Applicant reiterates its argument that Locke does not and cannot enablingly disclose the invention of the Applicant, and the rejection of claims 1-24 cannot stand.

CONCLUSION

Hence, Appellants respectfully request that all grounds of rejection be reversed.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayment to Deposit Account No. 50-0562 and notify the undersigned in due course.

Respectfully submitted,

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